

FDD7030BL/FDU7030BL

30V N-Channel PowerTrench® MOSFET

General Description

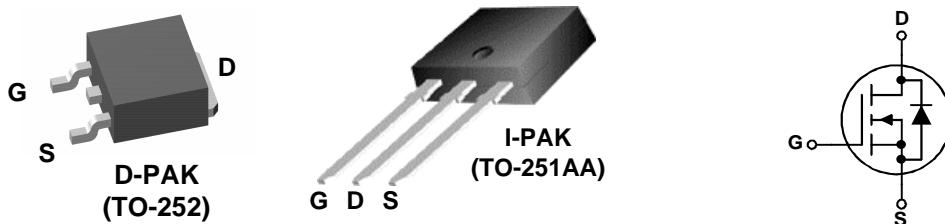
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

Applications

- DC/DC converter
- Motor Drives

Features

- 56 A, 30 V $R_{DS(ON)} = 9.5 \text{ m}\Omega$ @ $V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 13 \text{ m}\Omega$ @ $V_{GS} = 4.5 \text{ V}$
- Low gate charge
- Fast Switching
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current @ $T_C=25^\circ\text{C}$ (Note 3)	56	A
	@ $T_A=25^\circ\text{C}$ (Note 1a)	14	
	Pulsed (Note 1a)	100	
P_D	Power Dissipation @ $T_C=25^\circ\text{C}$ (Note 3)	60	W
	@ $T_A=25^\circ\text{C}$ (Note 1a)	2.8	
	@ $T_A=25^\circ\text{C}$ (Note 1b)	1.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	45	
$R_{\theta JA}$	(Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD7030BL	FDD7030BL	D-PAK (TO-252)	13"	12mm	2500 units
FDU7030BL	FDU7030BL	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
E_{AS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15\text{ V}$, $I_D = 14\text{ A}$			174	mJ
I_{AS}	Drain-Source Avalanche Current				14	A
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
ΔBV_{DSS} ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		26		$\text{mV/}^\circ\text{C}$
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$\Delta V_{GS(th)}$ ΔT_J	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-5		$\text{mV/}^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 12\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$, $T_J = 125^\circ\text{C}$	7.5 9.6 11	9.5 13 16		$\text{m}\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 14\text{ A}$		56		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		1425		pF
C_{oss}	Output Capacitance			350		pF
C_{rss}	Reverse Transfer Capacitance			150		pF
R_G	Gate Resistance	$V_{osc} = 15\text{ mV}$, $f = 1.0\text{ MHz}$		1.3		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		11	20	ns
t_r	Turn-On Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Turn-Off Fall Time			13	23	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}$, $I_D = 14\text{ A}$, $V_{GS} = 5\text{ V}$		14	20	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			5		nC

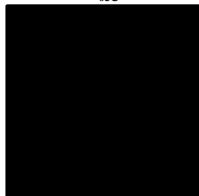
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.3		A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 2.3 \text{ A}$ (Note 2)	0.74	1.2		V
t_{rr}	Diode Reverse Recovery Time	$I_F = 14 \text{ A}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$	23			nS
Q_{rr}	Diode Reverse Recovery Charge		11			nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 45^\circ\text{C}/\text{W}$ when mounted on a
1 in² pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C}/\text{W}$ when mounted
on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as:

$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(ON)}$ is at $T_{J(\text{max})}$ and $V_{GS} = 10\text{V}$. Package current limitation is 21A

Typical Characteristics

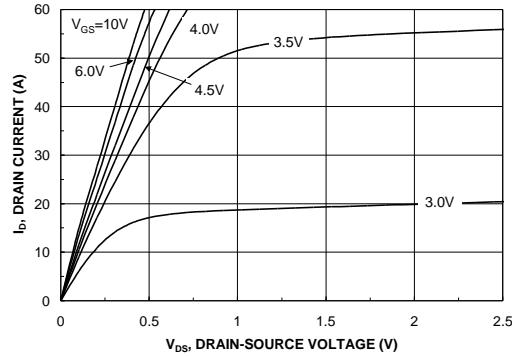


Figure 1. On-Region Characteristics

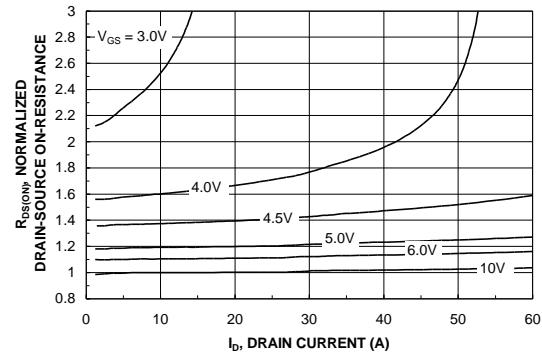


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

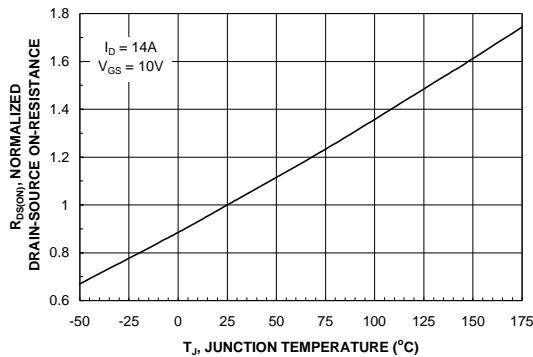


Figure 3. On-Resistance Variation with Temperature

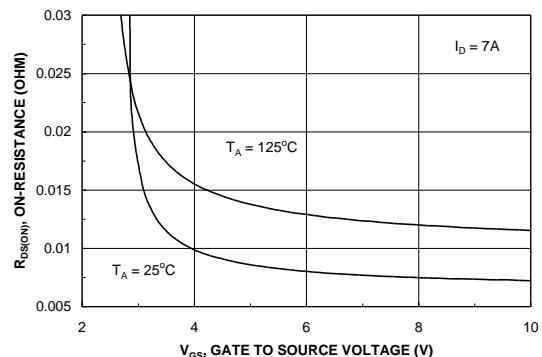


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

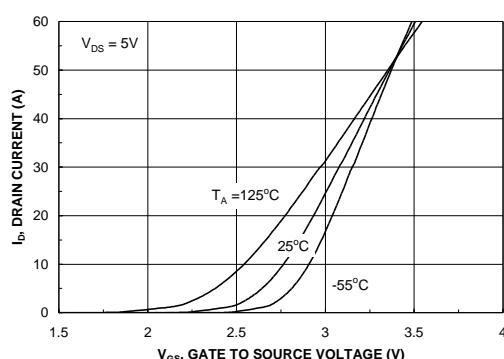


Figure 5. Transfer Characteristics

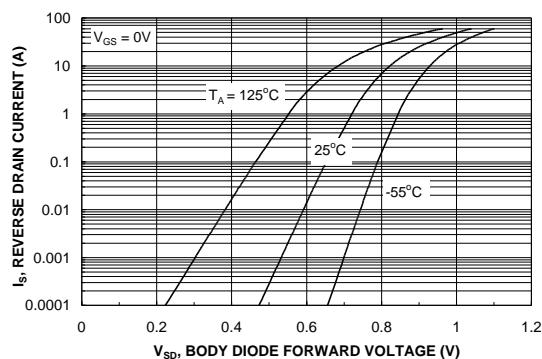


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

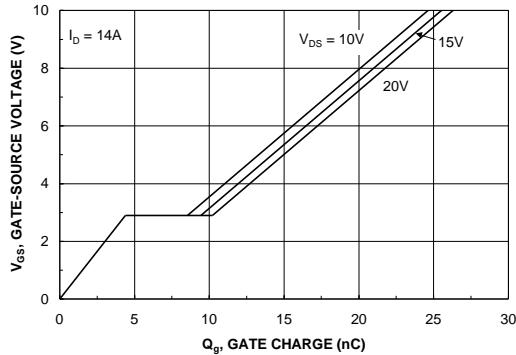


Figure 7. Gate Charge Characteristics

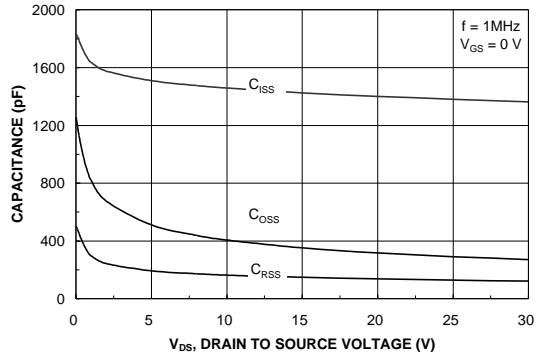


Figure 8. Capacitance Characteristics

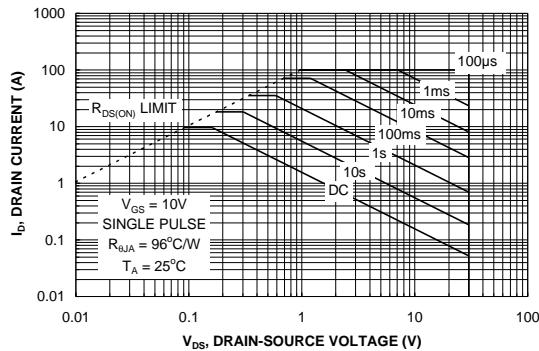


Figure 9. Maximum Safe Operating Area

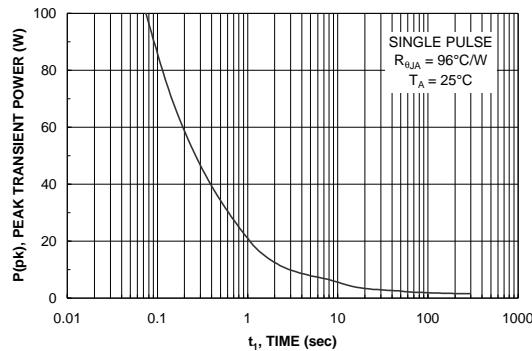


Figure 10. Single Pulse Maximum Power Dissipation

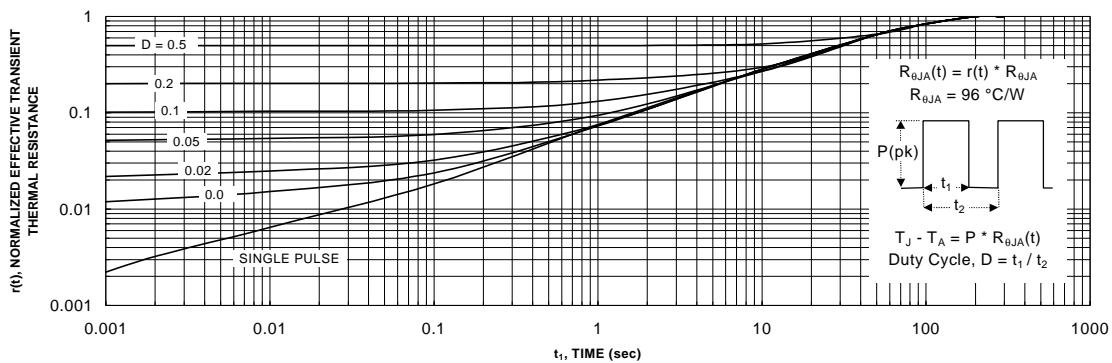


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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